Data Sheet

AS1130

30W Powered Device
With Integrated DC-DC Controller

Revision 0.9, October 2007

CONTENTS

GENERAL DESCRIPTION

The AS1130 is a single-chip, highly integrated CMOS solution designed for the emerging Power over Ethernet Plus (PoE+). Applications such include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security and Web Cameras and Point of Sales Terminals.

The AS1130 provides the functions required for power over Ethernet Powered Device (PD) applications. The device integrates a 100v, 800 mA MOSFET switch, a PD controller, and a DC-DC controller.

AS1130 has been designed to address 30W applications with reduced EMI emissions. The device implements many design features that minimizes transmission of system common-mode noise on to the UTP cable while providing high immunity to over-voltage and surge events.

By using high-volume standard CMOS technology, Akros enables its customers to implement higher performance PoE devices with low cost and a small footprint.

MAJOR FEATURES

The AS1130 is fully integrated and architected at a system level to provide the following features:

- Fully supports *IEEE*® Std. 802.3af-2003 and emerging 802.3at
- Complies with IEC 61000-4-2/3/4/5/6 requirements
- Complies with IEC 60950 overvoltage protection requirements
- Integrated DC-DC controller provides superior EMI performance
- Provides seamless support for local power
- Industrial temperature operating range, -40ºC to +85ºC
- Over-temperature protection
- 5x 5 mm, 20 lead QFN Package, RoHS compliant

TYPICAL APPLICATIONS

- Video & Voice over IP (VoIP) phones
- Wireless LAN Access Points
- Pan, Tilt and Zoom, security and Web Cameras
- Point of Sale (PoS)Terminals
- RFID Readers

EXAMPLE APPLICATION

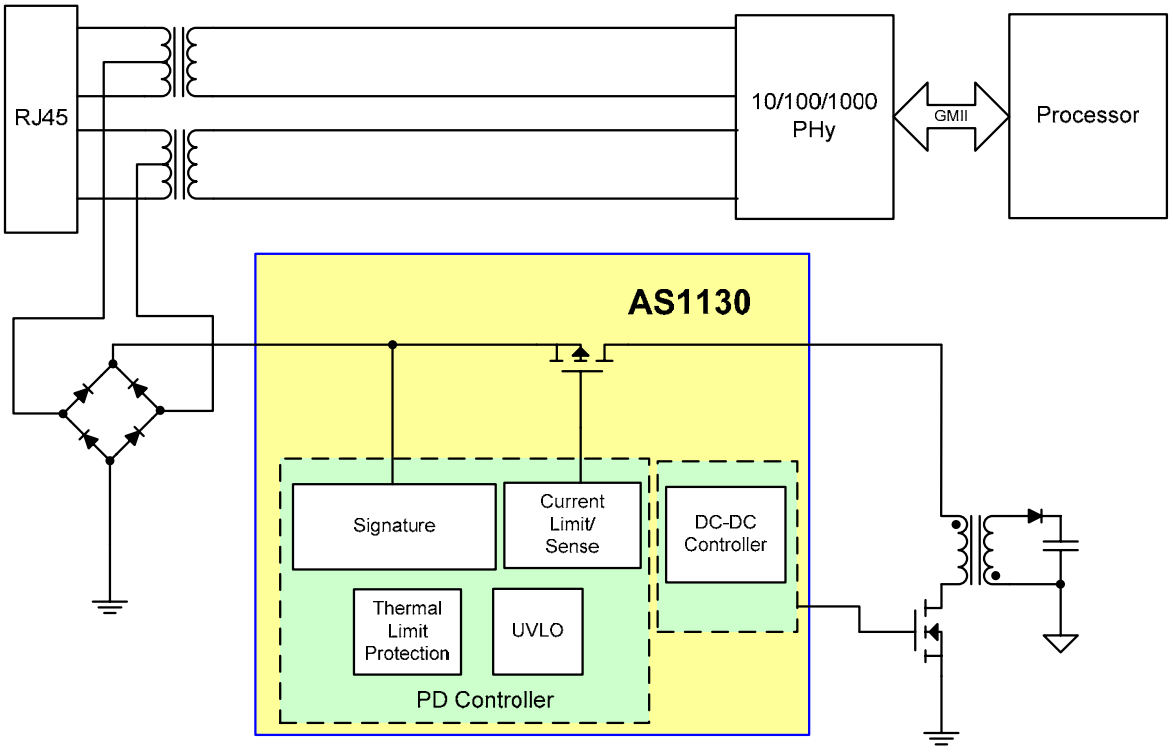


Figure 1. Typical Application Diagram for a PoE PD (Flyback Converter)

CONNECTION DIAGRAM

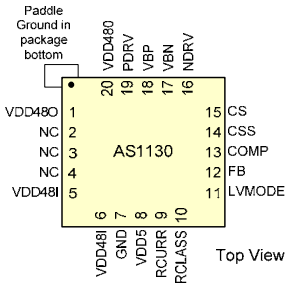


Figure 2. Pin-out Diagram

PIN DESCRIPTIONS

Table 1. Pin Assignments

Pin	I/O	Name	Description
1	P	VDD48O	Switched 48V supply output
2	-	N/C	No Connect
3	-	N/C	No Connect
4	-	N/C	No Connect
5	P	VDD48I	48V bus pin. This pin is the positive bus fed by the output of the input diode bridge. The bus requires the connection of an external ESD capacitor (82nF) and signature resistor (26.7kΩ).
6	P	VDD48I	
7	A	GND	Must be connected to paddle ground (not connected internally to the paddle).
8	A	VDD5	Internal 5 volts decoupling point
9	A	RCURR	Current limit pin. Connection to paddle ground sets the current limit to 400 mA. Open circuit sets the current limit to 800 mA
10	A	RCLASS	Classification resistor connection
11	A	LVMODE	Low Voltage Mode. When pulled high, LVMODE opens the internal FET switch and activates the DC-DC controller. Voltage threshold = 2.3 V
12	A	FB	DC-DC Controller feedback point
13	A	COMP	DC-DC Controller error amplifier compensation network connection
14	A	CSS	DC-DC Controller soft-start capacitor
15	A	CS	DC-DC Controller peak current sense input (low side)
16	O	NDRV	DC-DC Controller N-MOSFET gate drive
17	O	VBN	DC-DC Controller low side supply decoupling
18	O	VBP	DC-DC Controller high side supply decoupling
19	O	PDRV	DC-DC Controller P-MOSFET gate drive
20	P	VDD48O	Switched 48V supply output
Paddle	P	GND	Local ground. This is the negative output from the diode bridge, and is not isolated from the line input

Key:

I = Input
O = Output
I/O = Bidirectional

PD = Internal pull-down
A = Analog signal
P = Power

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings[1]

Unless otherwise noted, specifications are for T_a = -40°C to +85°C and V_{IN} = 48V.

Description	Max Value	Units
High voltage pins (5, 6—VDD48I; 18—VBP; 19—PDRV; 1, 20—VDD48O)	60	Volts
Low voltage pins (8—VDD5; 10—RCLASS; 12—FB; 13—COMP; 14—CSS; 15—CS; 16—NDRV; 17—VBN, 11-LVMODE)	6	Volts
ESD Rating:		
Human body model[2]	2	kV
ESD charged device model	500	V
System level (contact/air) at RJ-45	8/15	kV
Temperature		
Storage Temperature	165	°C
Junction Temperature	150	°C

[1] Absolute maximum ratings are limits beyond which damage to the device may occur.

[2] The human body model is as described in JESD22-A114.

NORMAL OPERATING CONDITIONS

Table 3. Normal Operating Conditions

Unless otherwise noted, specifications are for V_{in} = 48V operation

Description	Min	Typical[1]	Max
V_{in}	36V	48V	57V
Power dissipation (12V output at 2.1A)		1.7W	
Operating temperature range	-40°C		85°C

[1] Typical specification; not 100% tested. Performance guaranteed by design and/or other correlation methods.

KEY ELECTRICAL CHARACTERISTICS

Table 4. Electrical Characteristics

Unless otherwise noted, specifications are for T_a = -40°C to +85°C and V_{IN} = 48V.

	Min	Typical[1]	Max	Units	Comments
PD Section					
Inrush Current Limit		200		mA	Initial inrush current.
Current limit			800	mA	
Max. operating current		750		mA	
Switch R_{DS-ON}		1.25	1.5	Ω	Measured from VDD48I to VDD48O
Reset voltage level	0		2.7	V	
Min Signature voltage			2.7	V	
Max Signature voltage	10.1		14.5	V	
Min Classification voltage			14.5	V	In classification, the AS1130 sinks current as defined in table 5
Max Classification voltage	20.5			V	
Full power activation threshold	42			V	
Full power de-activation threshold	30		36	V	
DC-DC Controller Section					
F_{OSC} (SMPS) switching frequency	325	350	375	kHz	Controller operating frequency
F_{OSC} Temperature Coefficient		0.12		%/C	
PDRV R_{OUT}		1.5	4.5	Ω	High side output drive resistance
NDRV R_{OUT}		1.2	3	Ω	Low side output drive resistance
PDRV and NDRV Gate Drive V_{OH} - V_{OL}	4.5		6	V	
Gate Drive Dynamic Response PDRV T_R, T_F NDRV T_R, T_F		 2.2 2		 nS nS	10% - 90% with C_{Load} = 1 nF
V_{PK}, peak current sense threshold voltage at CS	500	600	700	mV	Ipeak=Vpk/Rsense
Max. duty cycle		80		%	Internally limited
Min. duty cycle		6		%	Internally limited
VBN		4.7		V	Low side internal supply voltage; sets V_{OH} of NDRV.
VBP (relative to VDD48O)		-5		V	High side internal supply voltage; sets V_{OL} of PDRV.
Error amplifier reference voltage	1.45		1.55	V	Compared to input of the FB pin
Soft start ramp time		2		ms	Conditions: CSS=100nF
COMP source current		30		µA	FB = 0V, COMP=0V
COMP sink current		30		µA	FB = 5V, COMP=5V
Open loop voltage gain		80		dB	

Table 4. Electrical Characteristics

Unless otherwise noted, specifications are for T_a = -40°C to +85°C and V_{IN} = 48V.

	Min	Typical[1]	Max	Units	Comments
Small signal unity gain bandwidth		5		MHz	COMP connected to FB.
FB leakage (source or sink)		1		µA	0V>FB>4.5V
Local Power Mode					
LVMODE Threshold	2.1		2.4	V	
LVMODE Hysteresis		100		mV	
LVMODE Operating Voltage	10		57	V	
Thermal Protection					
Thermal shutdown temperature		165		°C	Above this Temp., the AS1130 is disabled.
Max. on-die operating temperature		140		°C	
Current reduction temperature threshold		145		°C	Temperature at which thermal current reduction is applied
Thermal current reduction		50		%	
Thermal current reduction hysteresis		20		°C	Temperature change required to restore full operation after thermal current reduction
Thermal shutdown hysteresis		40		°C	Temperature change required to restore full operation after thermal shutdown

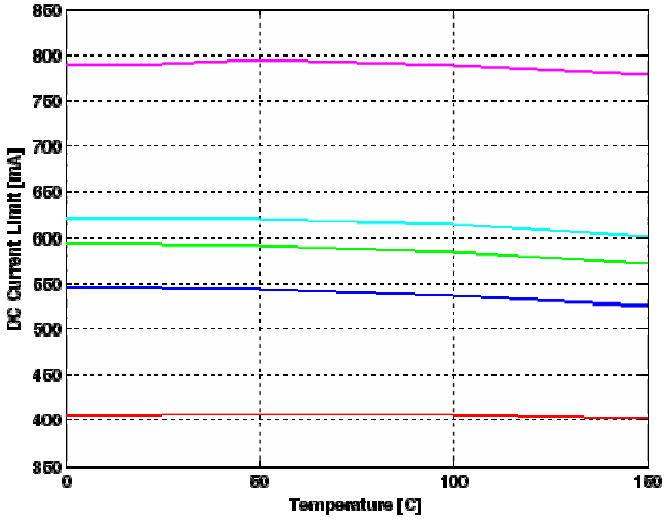
[1] Typical specifications are not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 5. Package Thermal Characteristic

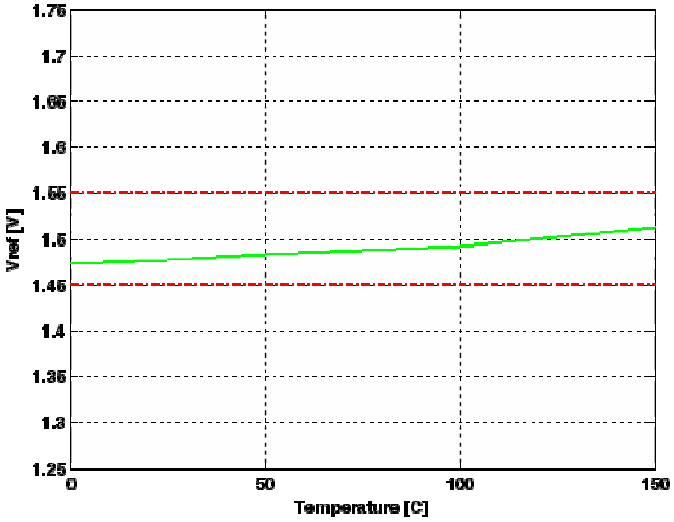
	Min	Typical[1]	Max	Units	Comments
Thermal Resistance, Junction to Ambient, [1] θ_{JA},		31		°C/W	20 lead QFN package
Power dissipation, P_{DISS}		1.7		W	25W Output, (12V output at 2.0A)

TYPICAL PERFORMANCE CHARACTERISTICS

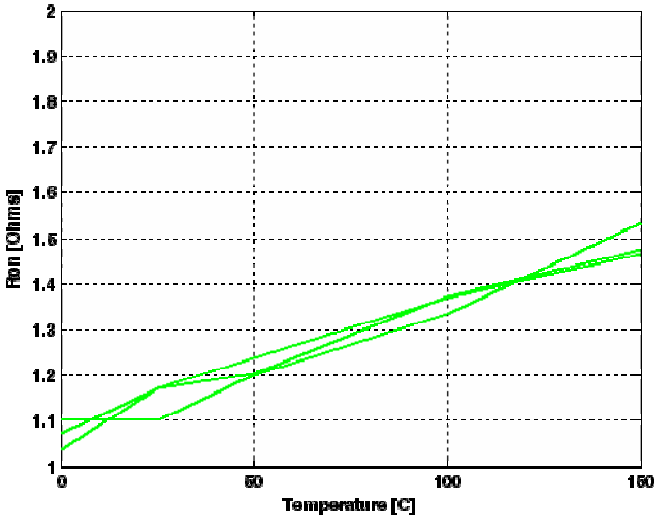
DC Current Limit vs. Junction Temp.[1]



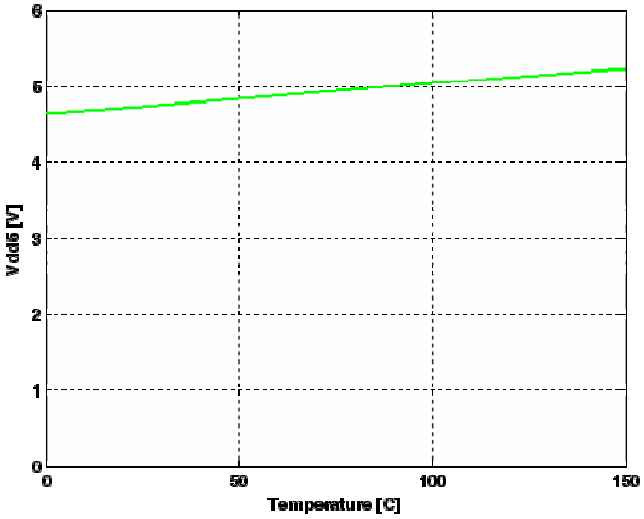
Error Amplifier Ref. Voltage vs. Junction Temp.



Switch R_{DS-ON} vs. Junction Temp. (Min/Max V_{IN})

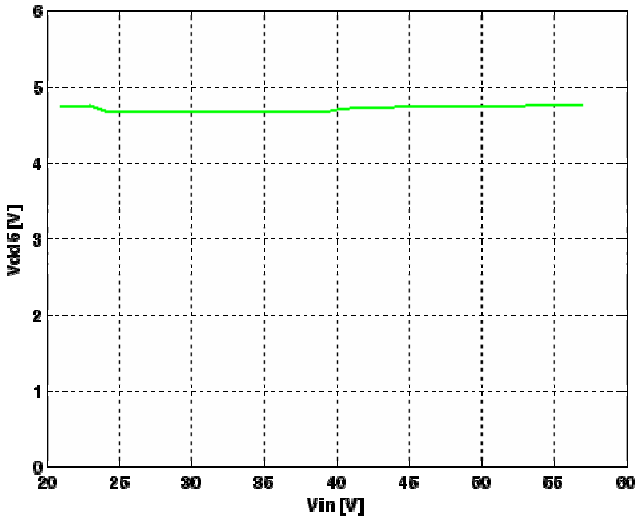


VDD5 vs. Junction Temp.

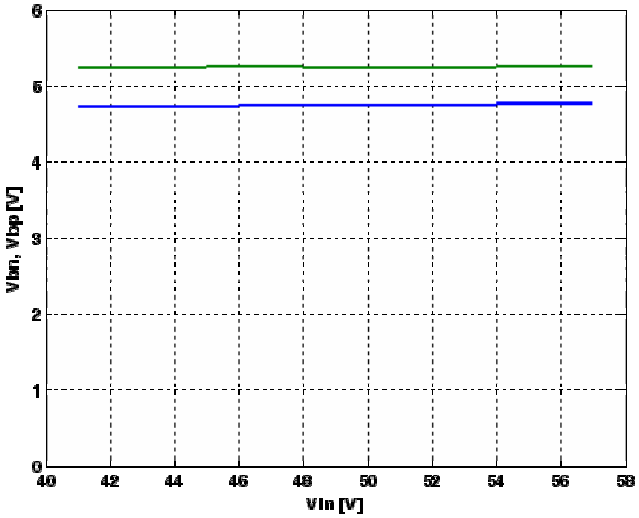


[1] [1] Current limit measured with RCURR= 0, 27kΩ, 47 kΩ, 67 kΩ and Open

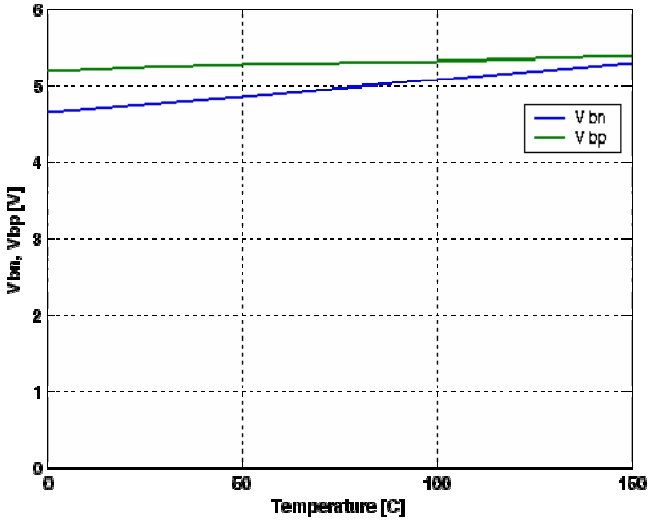
VDD5 vs. Vin



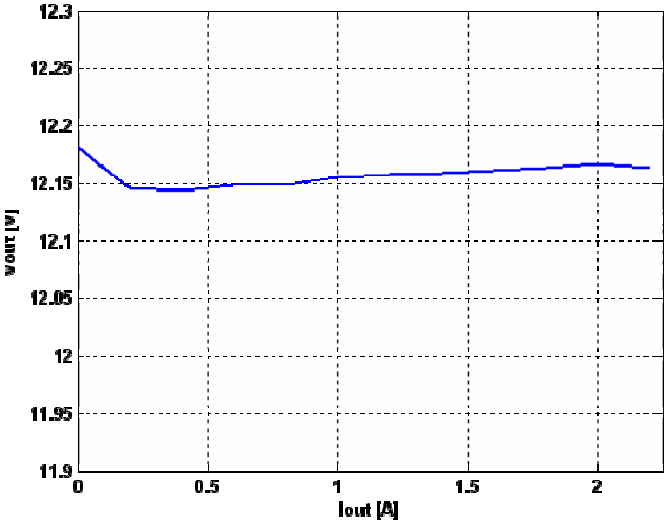
VBN & VBP (VBP wrt VDD48O) vs. Vin



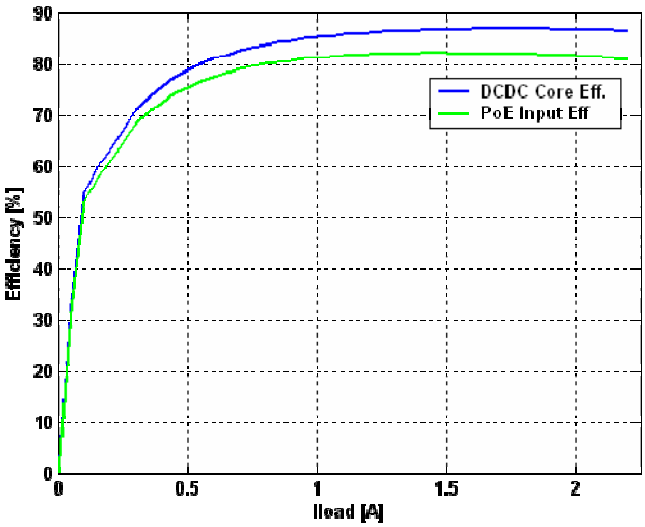
VBN & VBP (VBP wrt VDD48O) vs. Junction Temp.



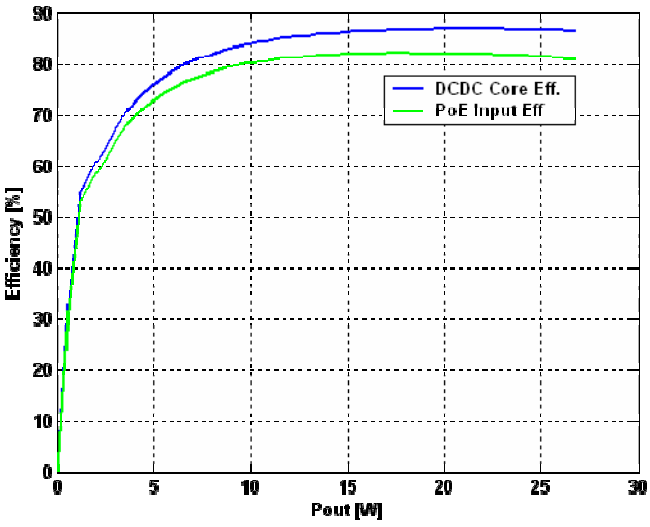
DCDC Load Regulation vs. I_{OUT} @V_{IN}=48V



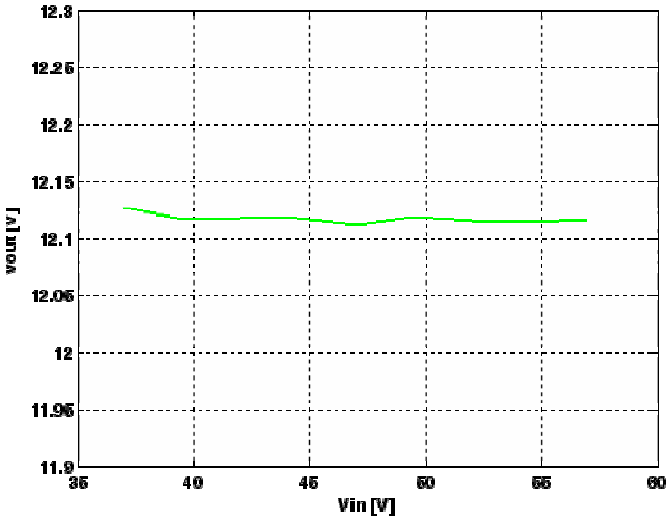
DCDC Efficiency vs. I_{OUT} @V_{IN}=48V, V_O=12v



DCDC Efficiency vs. P_{OUT} @ V_{IN}=48V, V_O=12v



DCDC Line Regulation @I_{OUT}=0.25A



FUNCTIONAL DESCRIPTION

OVERVIEW OF POE

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). The emerging PoE standard *IEEE*® Std. 802.3at is intended to standardize the delivery of power over the Ethernet cables in order to accommodate remotely powered client devices. The draft *IEEE*® Std. 802.3at r0.9 defines a method for recognizing PDs on the network and supplying different power levels according to power level *classes* with which each PD is identified. By employing this method, designers can create systems that minimize power usage, allowing more devices to be supported on an Ethernet network.

The end of the link that provides power through the Ethernet cables is referred to as the power sourcing equipment (PSE). The powered device (PD) is the end of the link that receives the power. The PoE method for recognizing a PD and determining the correct power level to allocate uses the following sequence:

- *Reset*, wherein power is withdrawn from the PD if the applied voltage falls below a specified level.
- *Signature Detection*, during which the PD is recognized by the PSE.
- *Classification*, during which the PSE reads the power requirement of the PD. The Classification level of a PD identifies how much power the PD requires from the Ethernet line. This permits optimum use of the total power available from the PSE.
- *ON* operation, during which the allocated level of power is provided to the PD.

This sequence occurs as progressively rising voltage levels from the PSE are detected.

To design PoE systems according to the PoE standard, designers have the following constraints:

Table 6. PoE Requirements

Requirement	Value
Maximum power to the PD interface	30 W
Voltage from Type 1 PSE	44-57V
Voltage from Type 2 PSE	50-57V
Maximum operating current	720mA
Line resistance	14Ω
Voltage drop due to series line resistance	10V
Min voltage at PD interface	40V

THE AS1130 PoE DESIGN

The AS1130 is a fully integrated PoE PD controller. The AS1130 meets all system requirements for the *IEEE*® 802.3 standard for Ethernet and all power management requirements for the emerging 802.3at standard. The device has been designed to receive a 30W input. Accounting for losses in the bridge diodes and integrated switch, the effective power delivered to the load is 25W. The Pulse Width Modulated (PWM) controller has been designed for low noise operation and EMI compliance has been verified for CISPR 22, FCC class B radiated emissions and EN55022 conducted emissions.

The AS1130 acts as the interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. Integrated surge protection provides protection during “hot” plug-in and other voltage spikes that may occur on the line. The AS1130 passes 2kV ESD tests, as well as 8kv Contact Discharge and 15 kV air Discharge tested per IEC61000-4.2,4.4,4.5.

Power Feed Alternatives for 10/100 Systems

Figure 3 illustrates the two power feed options allowed in the 802.3at standard for 10/100 systems. In Alternative A, a PSE powers the end station by feeding power along the twisted pair cable used for the 10/100 Ethernet signal via the center taps of Ethernet transformers. On the line side of the transformers for the PD, power is delivered through pins 1 and 2 and returned through pins 3 and 6. In Alternative B, a PSE powers the end station by feeding power through the cable pairs not used for 10/100 data transmission. Power is delivered through pins 4, 5, 7 and 8 without transformers.

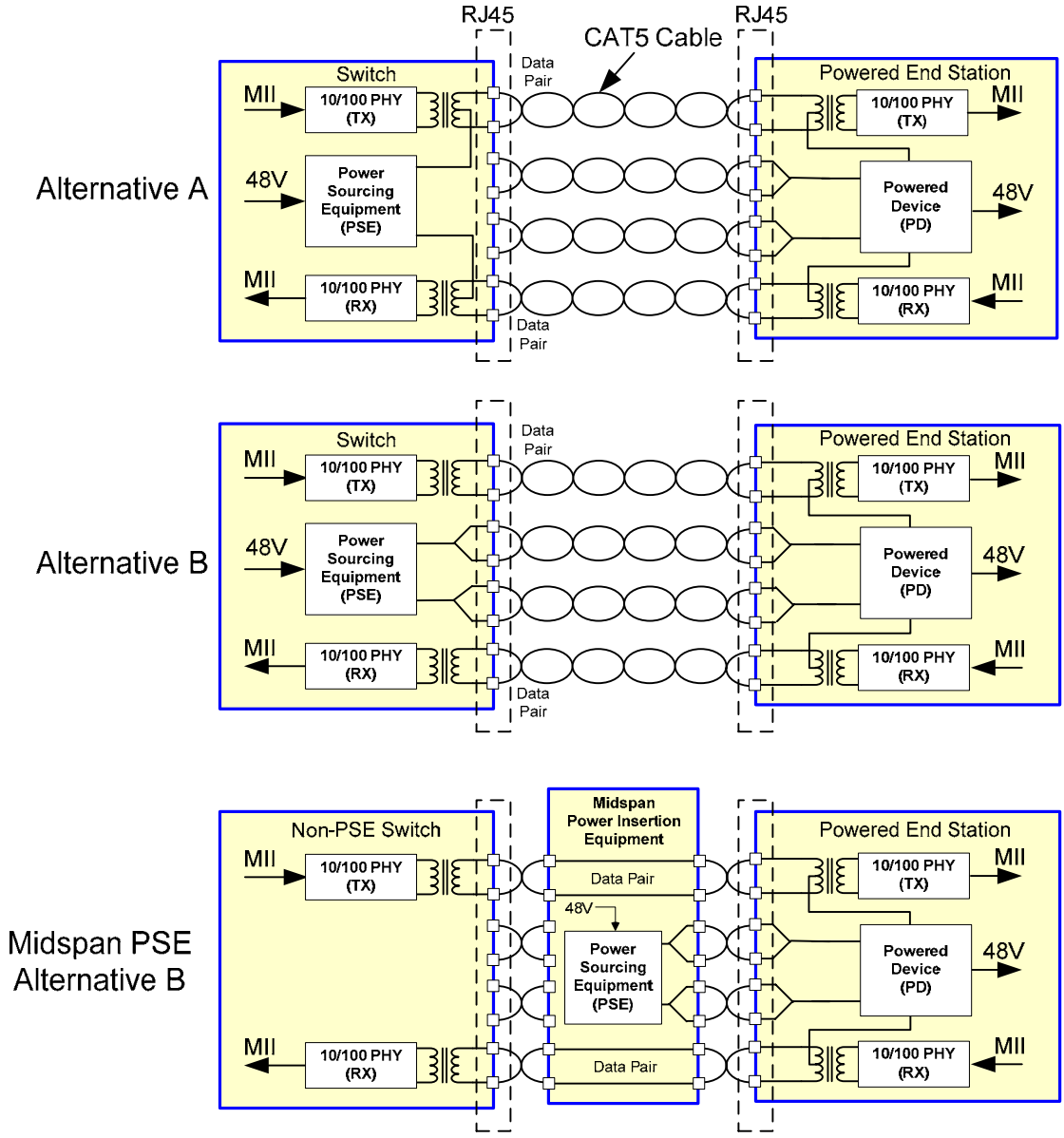


Figure 3. IEEE® Std. 802.3at Power Feeding Schemes for 10/100 Systems

The *IEEE*® Std. 802.3at is intended to be fully compliant with all existing non- powered Ethernet systems. As a result, the PSE is required to detect via a well-defined procedure whether or not the connected device is PD compliant and classify the needed power prior to applying power to the system. Maximum allowed voltage is 57V to stay within SELV (Safety Extra Low Voltage) limits.

AS1130 OVERVIEW

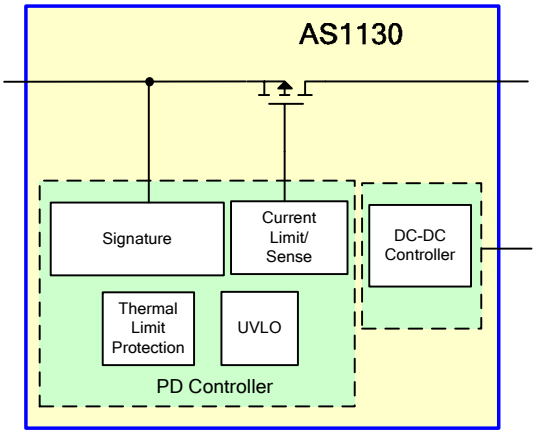


Figure 4. Top-Level Block Diagram of the AS1130

The AS1130 is a fully integrated PD that provides the functions required for power over Ethernet (PoE) applications. The optimized architecture of the AS1130 reduces external component cost in a small footprint while delivering high performance.

PD CONTROLLER

The AS1130 PD Control interface is designed to provide full PD functionality for IEEE 802.3at compliant systems, with programmable support for the standard PD control functions.

The PD Control provides the following major functions:

- Provides a resistance for signature detection.
- Provides classification currents for power classification.
- Provides PD full power.
- Manages power and thermal protection overrides, including UVLO (under voltage lockout).

Modes of Operation

The AS1130 has five operating modes:

- Reset— The classification state machine is reset, and all blocks are disabled.
- Signature Detection —The PD signature resistance is applied across the input.
- Classification—PD indicates power requirements to the PSE.
- Idle—This state is entered after classification, and remains here until full-power input voltage is applied.
- ON—The PD is enabled, and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the AS1130 transitions through the modes of operation in this sequence:

Reset ⇨ Signature Detection ⇨ Classification ⇨ Idle ⇨ ON

If no PSE is present, line voltage will be zero, which will hold the AS1130 in the reset state, and the AS1130 does not affect the Ethernet link function.

Reset

When the voltage supplied to the AS1130 drops below the signature voltage range (i.e. <2.7V), the chip will enter the reset state. In the reset state, the AS1130 consumes very little power.

Signature Detection Mode

During signature detection, the PSE applies a voltage to the AS1130 PD to read its power signature. The reading of the signature determines whether or not a PD is present and, if so, allows the PSE to determine the power class the PD belongs to.

To detect a PD, the PSE applies two voltages in the signature voltage range, and extracts a signature resistance value from the I-V slope. Valid resistance (I-V slope) values are between 23.75kΩ and 26.25kΩ. For the AS1130, signature resistance is generated by an external resistor between VDD48I and GNDA. Typically this is a 26.7kΩ resistor.

Classification Mode

Each class represents a power allocation level for a PD, so that PSE can manage power between multiple PDs. The emerging *IEEE*® Std. 802.3at defines classes of power levels for PDs as shown in Table 7.

To classify the PD, the PSE presents a voltage between 14.5V and 20.5V to the PD and determines its class by measuring the load current the PD sinks.

The AS1130 allows the user to program the classification current via an external resistor in the RCLASS pin. Current, power levels and programming resistor values for each class are shown in Table 7.

Use the following equation to determine typical classification current:

- $$I_{CLASS}[mA] = 2.0 + \frac{2360}{R_{CLASS}[k\Omega]}$$
- Tolerance = Maximum of ±1.8mA or ±9%
- R_{CLASS} > 63.4kΩ

Table 7. Classification Map

Class	Power (Watts)	Iclass	Rclass
0	0.44-12.95	0-4 mA	Pull-up / Open
1	0.44-3.84	9-12 mA	280kΩ
2	3.84-6.49	17-20 mA	143kΩ
3	6.49-12.95	26-30 mA	90.9kΩ
4	12.96-30	36-44 mA	63.4kΩ

Local Power Mode

The LV Mode Pin can be used in applications where the PD appliance draws power from either the Ethernet cable or an external DC power source. When pin 6 is pulled high (> 2.3V), it will open the internal FET switch while the DC-DC converter remains operational. The auxiliary power should be injected at the VDD48O node, through an external Schottky diode. Refer to application circuits 8 & 9 for the connection details.

The maximum input voltage at the LVMODE pin should not exceed 6V. A resistive divider network should be used to divide down the LVMODE control voltage. The internal DC-DC converter will operate with input voltages ranging from 10V to 57V. Depending on voltage level of the auxiliary adapter, the resistive divider should be scaled to assure that the LVMODE control voltage does not exceed 6V.

If the LVMODE pin is pulled low, the PD will operate in a normal fashion, whereby the FET will open when the input voltage at VDD48I drops below 36V.

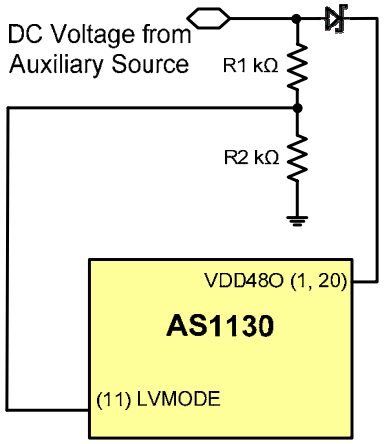
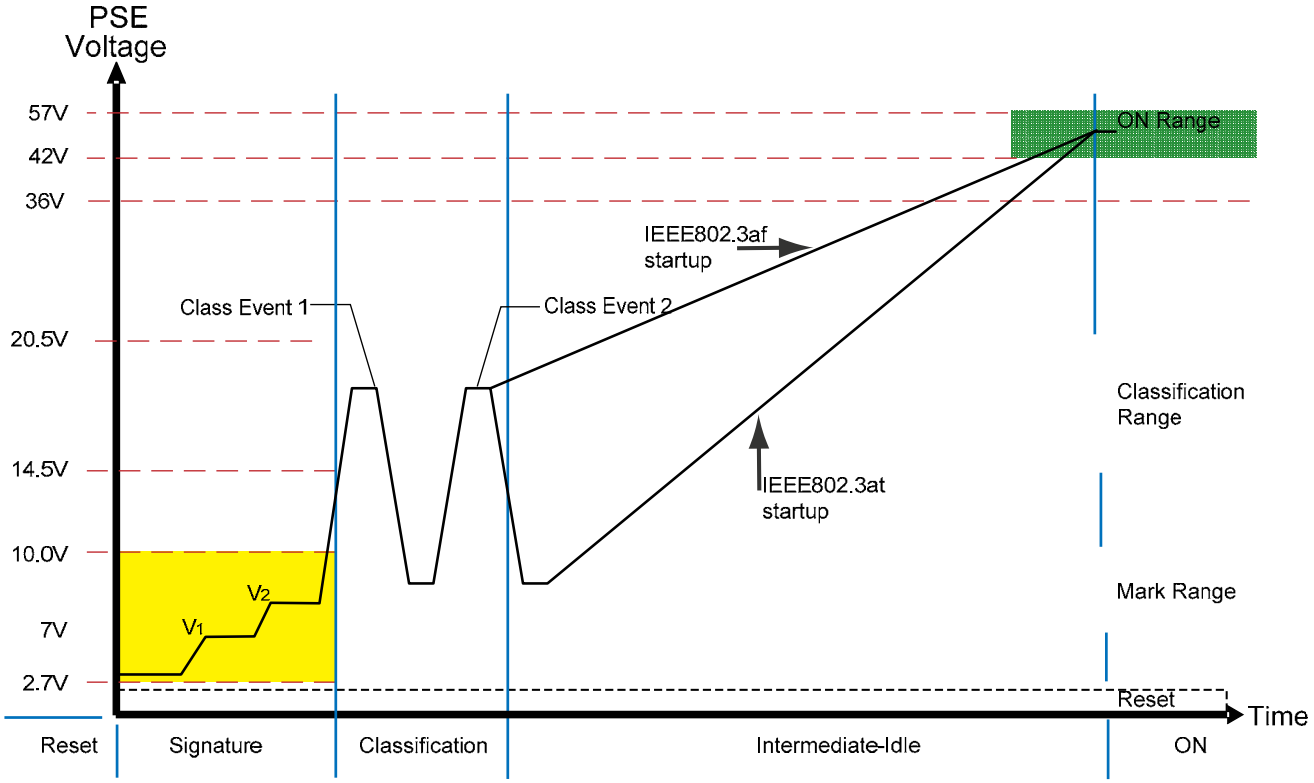


Figure 5. AS1130 LVMODE Connection

PoE Power-On Startup Waveform

Figure 6 represents the power-on sequence for PoE operation. The waveform reflects typical voltages present at the PD-PI during signature, classification and power-on.



Notes

1. Voltages V1 and V2 are applied by a PSE to extract a signature resistance value.
2. The PSE takes current readings during Class Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistance on the RCLASS pin.
3. After the PSE measures the PD load current, if it is a high power PSE it presents a mark voltage (between 7V and 10V) followed by a second classification. The PD responds by presenting a load current as determined by the resistor on the RCLASS pin. After the PSE measures the PD load current the second time, and determines that it can deliver the requested power, it moves into the ON state by raising the voltage above 42V.

Figure 6. Representative Power-On waveform

Idle Mode

In the Idle mode, between Classification and the ON state, PD Current is limited to monitoring circuitry to detect the on-state threshold.

ON State

In the ON state, the AS1130 is supplying power.

At a voltage at or above 42V, the PD turns on and full power is available via the AS1130 DC-DC Controller.

PD CONTROL POWER AND THERMAL PROTECTIONS

The AS1130 provides the following PD control power and thermal protections:

- Under Voltage Lockout (UVLO)
- Current Limit with integrated current sense
- Thermal Limit/Protection

Under Voltage Lockout (UVLO)

The AS1130 contains a line Under-Voltage Lockout (UVLO) circuit. The UVLO circuitry detects conditions when the supply voltage is too low (less than 36V), and disconnects the power to protect the PD.

Current Limit/Current Sense

The Current Limit/Current Sense circuitry minimizes on-chip temperature peaks by limiting inrush current and operating current. It monitors the current via an integrated sense circuit and regulates the gate voltage on an integrated low-leakage 80V power MOSFET. In addition, the power MOSFET can be shut down by the PD Controller subsection or the Thermal Limit Protection subsection.

Thermal Limit Protection

The AS1130 provides thermal protection for itself by monitoring die temperature and reducing maximum current or disconnecting power as needed to prevent pre-set thermal limits from being exceeded.

Two-stage thermal current limiting is implemented, which reduces the operating current limit by 50% when the die temperature reaches 145˚C, and disables the power MOSFET switch above 165˚C. Normal current limits in both cases are reapplied when the die temperature returns to 125˚C.

DC-DC CONTROLLER

Overview

The DC-DC architecture is a current-mode controller which can be configured with external component changes to flyback, forward, or non-synchronous low-side switch buck topologies. Both non-isolated and isolated topologies are supported.

The integrated DC-DC controller operates from a switched input voltage (VDD48O) and includes soft-start and current limiting. Once input power is applied and enable signals are asserted, the DC-DC controller starts up. The controller provides gate control signals to external switching MOSFETs, and uses an external resistor to sense the transformer primary current.

The DC-DC controller includes programmable soft start, 80% maximum duty cycle, fixed switching frequency and a voltage output error amplifier.

Current-Limit/Current Sense

The DC/DC controller provides cycle-by-cycle current limiting to ensure that transformer primary current limits are not exceeded. In addition, the maximum average current in the transformer primary is set by internal duty cycle limits.

Low Load Current Operation

The internal circuitry detects a low output power condition and puts the DC-DC Controller into a discontinuous current operation (DCM) mode.

Compensation and Feedback

For isolated applications, loop compensation and output voltage feedback is generally provided by an opto-isolator circuit, and the FB pin is shorted to ground. In these applications, the COMP pin is pulled up to 4.8V (nominally) by an internal current source. This pull-up can be the termination for an opto-isolator, or an additional resistor can be used in parallel.

For non-isolated applications, a resistive divider network senses the output voltage and is applied directly to the FB pin. The internal error amplifier is connected to a 1.5V reference voltage and the control loop will servo the FB pin to this voltage. A capacitive/resistive network connected to the COMP pin provides loop compensation.

Soft-Start inrush current limit

The internal circuitry automatically ramps up the inrush current by limiting the maximum current allowed in the transformer primary magnetizing inductance per clock cycle. The amount of time required to perform a soft start cycle is determined by the CSS capacitor. A CSS capacitor of 100 nF provides approximately 2ms of soft startup ramp time.

AUXILIARY POWER OPTION

The Auxiliary Power Option allows the AS1130 to be powered from a DC power source, other than the Ethernet line. Examples of DC sources are AC/DC wall adapters, batteries, or solar cells. This feature may also be used, to supply power that exceeds the load capacity of the PSE, or in non PoE systems.

DC-DC CONVERTER TOPOLOGIES

Flyback vs. Forward Operation

The DC-DC controller can be configured in several different operational topologies and in either isolated or non-isolated configurations. The FLYBACK mode is chosen when a minimum number of external components is desired or there is a large step-down and the output voltage is < 7V. The FORWARD mode is chosen with lower output noise and higher efficiency is desired. The FLYBACK mode is shown in Figure 8 and the FORWARD mode in shown in Figure 9, both in isolated configurations.

Buck Operation

The BUCK mode is shown in Figure 10. The buck mode is used only in non-isolated applications. The BUCK mode uses an inductor instead of a transformer and therefore has the smallest overall footprint. In Figure 10 the BUCK converter output voltage is referenced to VDD48O. Since the FB voltage is ground referenced, the feedback signal must be level shifted

back down to ground. This is accomplished by the two PNP transistors and the associated resistors.

Primary Switching Topology

The DC-DC controller uses a two-switch topology to minimize noise, maximize efficiency and reduce the breakdown requirements for the switching transistors. During OFF time and when the core is being reset, a snubbing circuit, consisting of parallel Schottky diodes, directs the transformer magnetizing current into the bulk storage capacitors connected to VDD48O. This additional snubbing circuitry minimizes the ringing that can occur on the primary winding of the power transformer. In single switch topologies, the maximum V_{DS} is approximately 2.5X VDD48O and there can be significant ringing during OFF time, when the transformer core is being reset. Again, snubbing circuitry is used to dissipate the ringing noise that occurs during the switching transitions.

Thermal De-rating and Board Layout Considerations

The AS1130 is capable of operating to industrial temperature range of 85 ºC, in ambient air and without forced cooling. A thermal pad on the underside of the package dissipates heat generated by the PD die. The designer must consider thermal design as an integral part of their systems design and remove heat via this pad.

When the PCB landing pattern is properly designed, the QFN package should exhibit a thermal resistance of Θ_{JA}=31°C/W.

For adequate heat dissipation, the board layout must include a ground pad which accomplishes both the ground connection and dissipates the heat energy generated by the PD. Thermal vias are used to draw heat away form the PD package and to transfer it to the backside of the system PCB

The recommended PCB layout for the AS1130 is shown in 7 below.

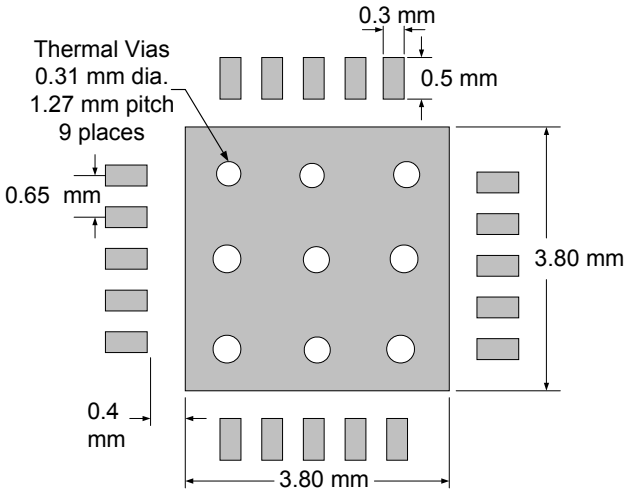
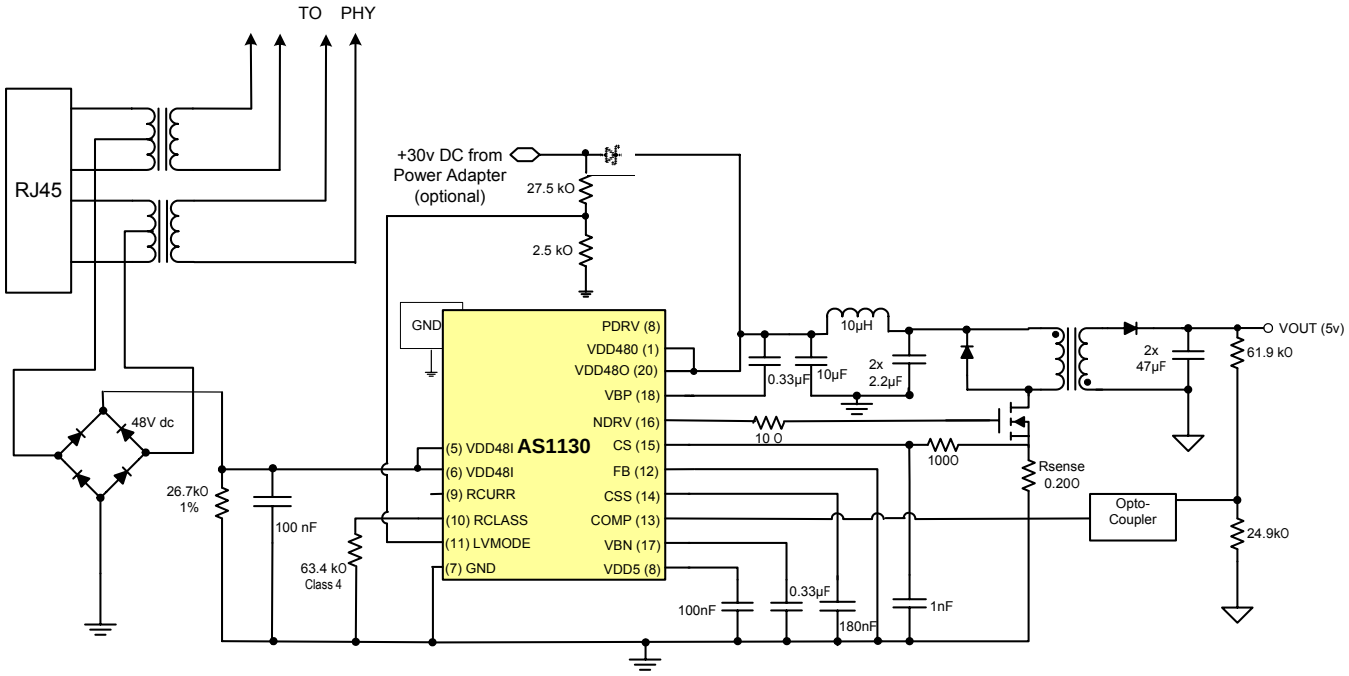


Figure 7. AS1130 PCB Footprint

APPLICATION CIRCUITS

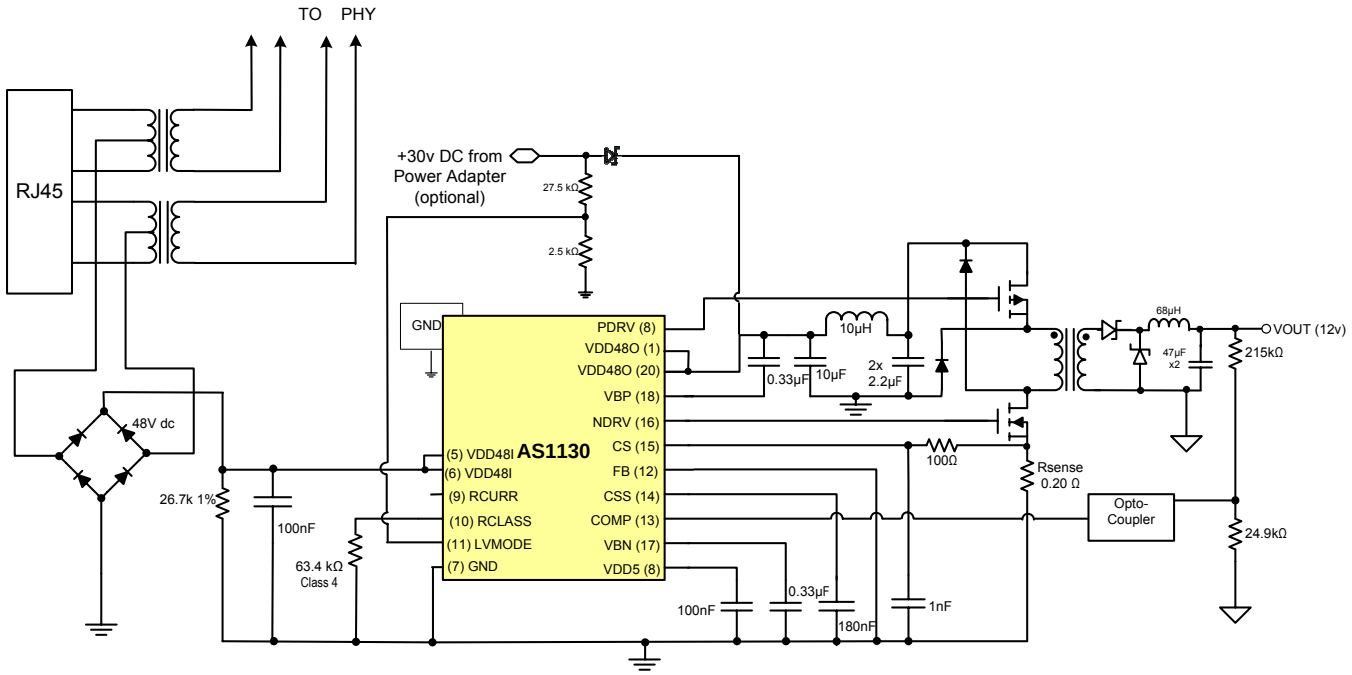
FIGURE 8. 10/100M WITH FLYBACK DC-DC CONVERTER



NOTES:

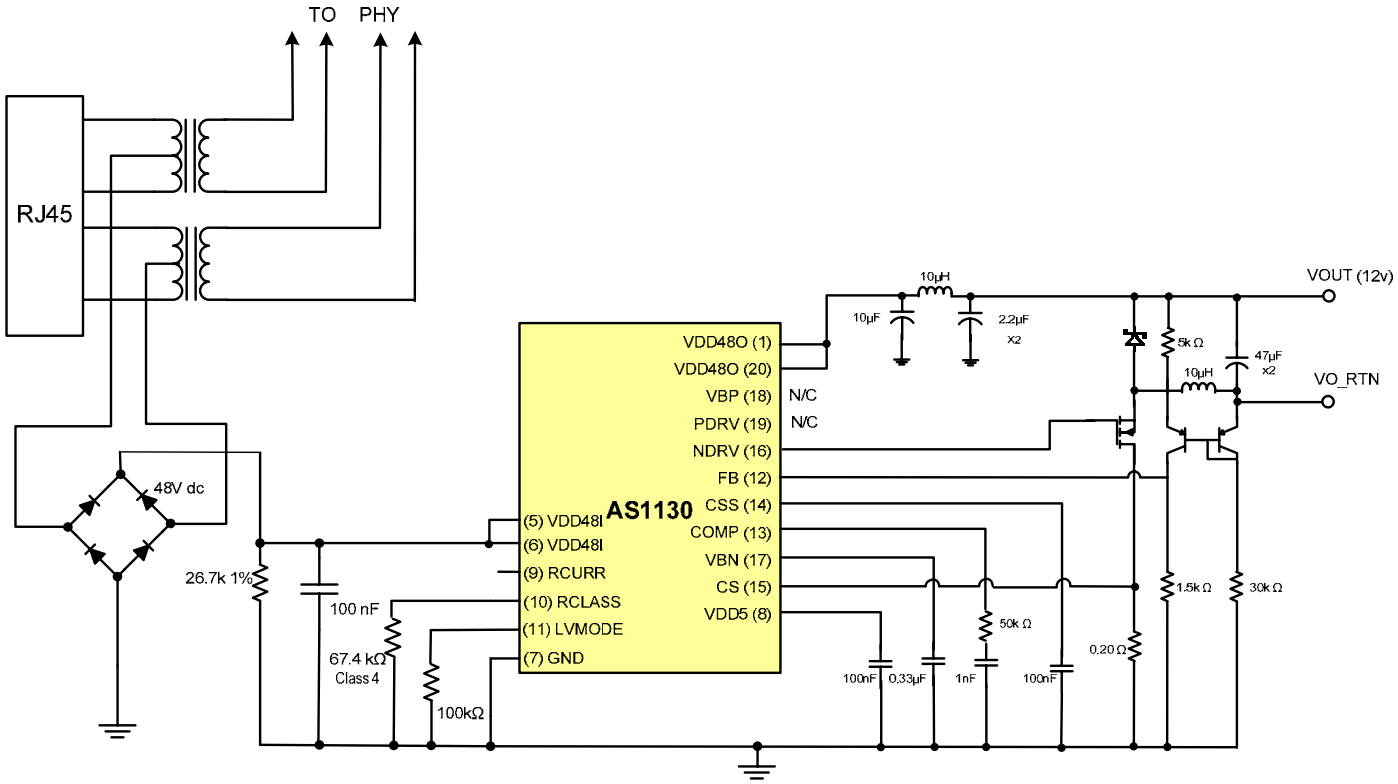
All resistors 1% except as otherwise noted
1. Dual FET: Vishay Si7530
2. T1: Transtek POET0076. For applications that use local power < 30 V DC, work with the transformer manufactures to optimize the windings for low voltage operation
3. Primary side Schottky diodes: B1100-13
4. Secondary Side Schottky diodes: SS36
5. Opto-Coupler FOD2712

FIGURE 9. 10/100M WITH FORWARD DC-DC CONVERTER



NOTES:
1. All resistors 1% except as otherwise noted
2. Dual FET: Vishay Si7530
3. T1: Transtek POET0062. For applications that use local power < 30 V DC, work with the transformer manufactures to optimize the windings for low voltage operation
4. Primary side Schottky diodes: B1100-13
5. Secondary Side Schottky diodes: SS36
6. Opto-Coupler FOD2712

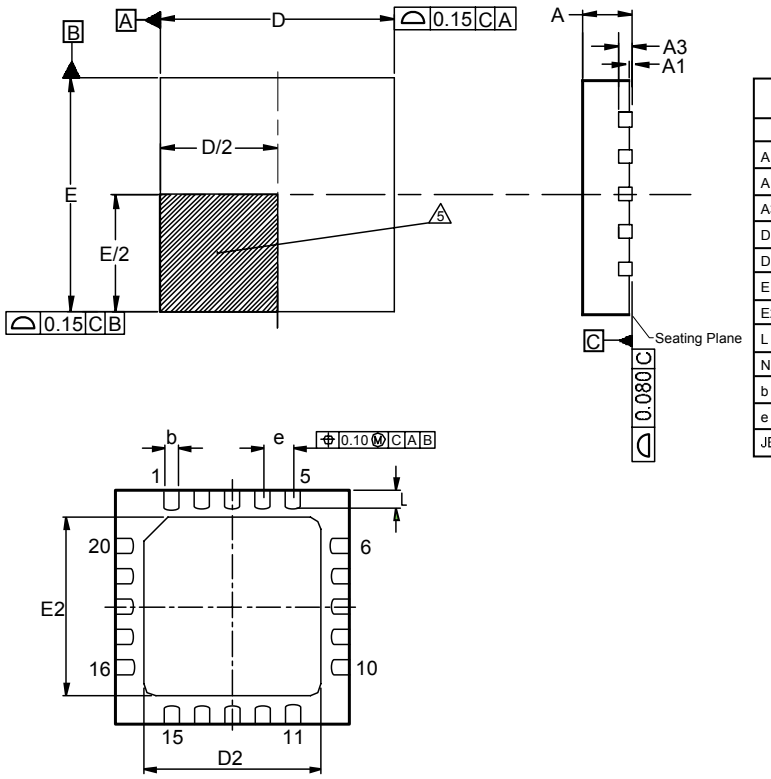
FIGURE 10. 10/100M WITH BUCK DC-DC CONVERTER



Notes:
All resistors 1% except as otherwise noted.
FET: Vishay Si7812
Schottky diode: MBR3203T3
PNP transistors: BC556

PHYSICAL DIMENSIONS

20 Pin QFN Package, 5mm X 5mm



Common Dimensions			
	MIN.	NOM.	MAX
A	0.80	0.85	0.95
A1	0.00	0.02	0.04
A3		0.20 REF.	
D	4.85	5.00	5.15
D2	3.70	3.80	3.90
E	4.85	5.00	5.15
E2	3.70	3.80	3.90
L	0.35	0.40	0.45
N		20L	
b	0.25	0.30	0.35
e		0.650 BSC	
JEDEC		MO-220-VHHC-2	

NOTES
1. Controlling dimensions in mm.
2. Dimension tolerances are ±0.1 (angular tolerance ±3˚) unless otherwise specified.
3. All dimensions and tolerances conform to ANSI Y14.5M-1994.
4. Coplanarity applies to exposed pad as well as the terminals.
5. Pin 1 location may be identified by either a mold or marked feature.
6. JEDEC reference MO-220.

CONTACT INFORMATION

Akros Silicon Inc.

275 Turn Pike Drive

Folsom, CA. 95630

USA

Tel: (916) 351-8100

Fax: (916) 351-8102

Email inquiries: marcom@akrossilicon.com

Website: www.akrossilicon.com

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